FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11237-1E

*MEMORY*

# 1 M × 32 BIT FAST PAGE MODE DRAM MODULE

# MB8501D032AA-60/-70

**72-pin SIMM, 1 M × 32 BIT Fast Page Mode DRAM Module, 5 V, 1-Bank**

## ■ DESCRIPTION

The Fujitsu MB8501D032AA is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of two MB8118160A devices. The MB8501D032AA is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB8501D032AA are the same as the MB8118160A which features fast page mode operation. For ease of memory expansion, the MB8501D032AA is offered in a 72-pad Single In-line Memory Module package (SIMM).

## ■ PRODUCT LINE & FEATURES

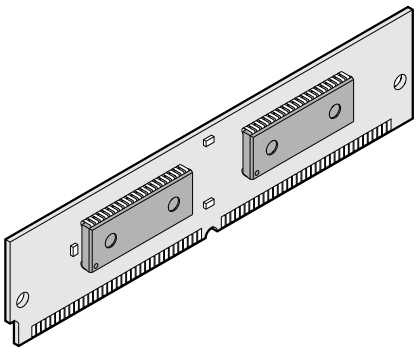
| Parameter | | MB8501D032AA | |
|---|---|---|---|
| | | -60 | -70 |
| $\overline{RAS}$ Access Time | | 60 ns max. | 70 ns max. |
| Random Cycle Time | | 110 ns min. | 130 ns min. |
| Address Access Time | | 30 ns max. | 35 ns max. |
| $\overline{CAS}$ Access Time | | 15 ns max. | 17 ns max. |
| Fast Page Mode Cycle Time | | 40 ns min. | 45 ns min. |
| Power Dissipation | Operating Mode | 1760 mW max. | 1650 mW max. |
| | Standby Mode | 11 mW (CMOS)/22 mW (TTL) | |

- Organization: 1,048,576 words × 32 bits
- Memory: MB8118160A, 2 pcs
- 5.0 V±10% Supply Voltage
- 1,024 Refresh Cycles/16.4 ms
- Self refresh capability
- Fast page mode operation
- Package and Ordering Information:
  72-pin SIMM, order as
  MB8501D032AA-××SG
  (SG = Gold Pad)

# MB8501D032AA-60/-70

## ■ PACKAGE

Plastic SIMM Package



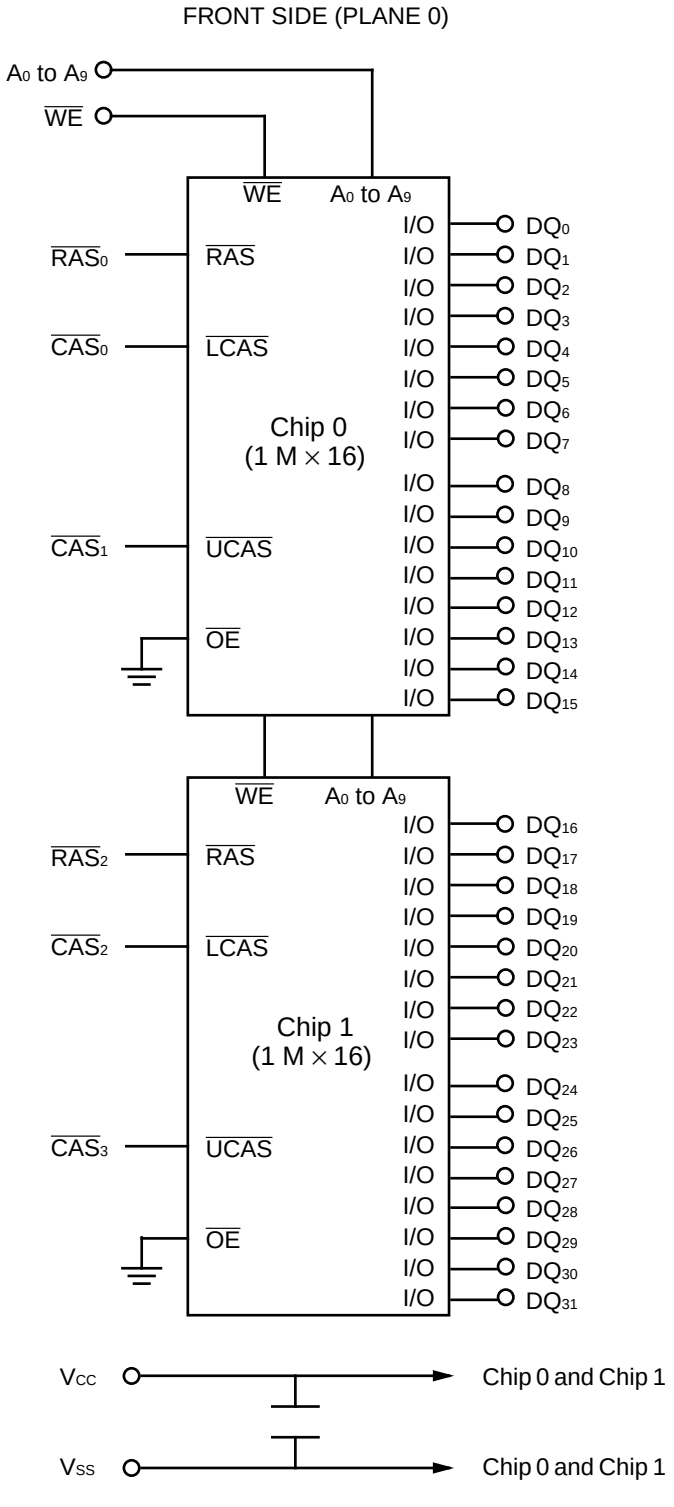
(MSS-72P-P86)

| | | | |
|---|---|---|---|
| $DQ_0$ | 2 | 1 | $V_{SS}$ |
| $DQ_1$ | 4 | 3 | $DQ_{16}$ |
| $DQ_2$ | 6 | 5 | $DQ_{17}$ |
| $DQ_3$ | 8 | 7 | $DQ_{18}$ |
| $V_{CC}$ | 10 | 9 | $DQ_{19}$ |
| $A_0$ | 12 | 11 | N.C. |
| $A_2$ | 14 | 13 | $A_1$ |
| $A_4$ | 16 | 15 | $A_3$ |
| $A_6$ | 18 | 17 | $A_5$ |
| $DQ_4$ | 20 | 19 | N.C. |
| $DQ_5$ | 22 | 21 | $DQ_{20}$ |
| $DQ_6$ | 24 | 23 | $DQ_{21}$ |
| $DQ_7$ | 26 | 25 | $DQ_{22}$ |
| $A_7$ | 28 | 27 | $DQ_{23}$ |
| $V_{CC}$ | 30 | 29 | N.C. |
| $A_9$ | 32 | 31 | $A_8$ |
| $\overline{RAS}_2$ | 34 | 33 | N.C. |
| N.C. | 36 | 35 | N.C. |
| N.C. | 38 | 37 | N.C. |
| $\overline{CAS}_0$ | 40 | 39 | $V_{SS}$ |
| $\overline{CAS}_3$ | 42 | 41 | $\overline{CAS}_2$ |
| $\overline{RAS}_0$ | 44 | 43 | $\overline{CAS}_1$ |
| N.C. | 46 | 454 | N.C. |
| N.C. | 48 | 7 | $\overline{WE}$ |
| $DQ_{24}$ | 50 | 49 | $DQ_8$ |
| $DQ_{25}$ | 52 | 51 | $DQ_9$ |
| $DQ_{26}$ | 54 | 53 | $DQ_{10}$ |
| $DQ_{27}$ | 56 | 55 | $DQ_{11}$ |
| $DQ_{28}$ | 58 | 57 | $DQ_{12}$ |
| $DQ_{29}$ | 60 | 59 | $V_{CC}$ |
| $DQ_{30}$ | 62 | 61 | $DQ_{13}$ |
| $DQ_{31}$ | 64 | 63 | $DQ_{14}$ |
| N.C. | 66 | 65 | $DQ_{15}$ |
| $PD_2$ | 68 | 67 | $PD_1$ |
| $PD_4$ | 70 | 69 | $PD_3$ |
| $V_{SS}$ | 72 | 71 | N.C. |

| Pin # | Symbol | -60 | -70 |
|---|---|---|---|
| 67 | $PD_1$ | $V_{SS}$ | $V_{SS}$ |
| 68 | $PD_2$ | $V_{SS}$ | $V_{SS}$ |
| 69 | $PD_3$ | N.C. | $V_{SS}$ |
| 70 | $PD_4$ | N.C. | N.C. |

# MB8501D032AA-60/-70

**Fig.1 – BLOCK DIAGRAM**



# MB8501D032AA-60/-70

## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | –0.5 to +7.0 | V |
| Input Voltage | $V_{IN}$ | –0.5 to +7.0 | V |
| Output Voltage | $V_{OUT}$ | –0.5 to +7.0 | V |
| Short Circuit Output Current | $I_{OUT}$ | –50 to +50 | mA |
| Power Dissipation | $P_D$ | 2 | W |
| Storage Temperature | $T_{STG}$ | –55 to +125 | °C |

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

**(Referenced to $V_{SS}$)**

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Ground | $V_{SS}$ | 0 | 0 | 0 | V |
| Input High Voltage, All Inputs | $V_{IH}$ | 2.4 | — | 6.5 | V |
| Input Low Voltage, All Inputs* | $V_{IL}$ | –0.3 | — | 0.8 | V |
| Ambient Temperature | $T_A$ | 0 | — | 70 | °C |

**Note:** * Undershoots of up to –2.0 volts with a pulse width not exceeding 20 ns are acceptable.

**WARNING:** Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

## ■ CAPACITANCE

($T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0 V)

| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | Typ. | Max. | |
| Input Capacitance, $A_0$ to $A_9$ | $C_{IN1}$ | — | 30 | pF |
| Input Capacitance, $\overline{RAS}_0$ and $\overline{RAS}_3$ | $C_{IN2}$ | — | 12 | pF |
| Input Capacitance, $\overline{CAS}_0$ to $\overline{CAS}_3$ | $C_{IN3}$ | — | 13 | pF |
| Input Capacitance, $\overline{WE}$ | $C_{IN4}$ | — | 21 | pF |
| I/O Capacitance, ($DQ_0$ to $DQ_{31}$) | $C_{DQ}$ | — | 24 | pF |

## ■ DC CHARACTERISTICS

**(At recommended operating conditions unless otherwise noted.)**

| Parameter | Notes | | Condition | Symbol | Value | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min. | Max. | |
| Output High Voltage | *1 | | $I_{OH}$ = –5 mA | $V_{OH}$ | 2.4 | — | V |
| Output Low Voltage | *1 | | $I_{OL}$ = 4.2 mA | $V_{OL}$ | — | 0.4 | V |
| Input Leakage Current | | $\overline{RAS}$ | 0 V ≤ $V_{IN}$ ≤ $V_{CC}$, 4.5 V ≤ $V_{CC}$ ≤ 5.5 V, $V_{SS}$ = 0 V, all other pins not under test = 0 V | $I_{I(L)}$ | –20 | 20 | µA |
| | | $\overline{CAS}$ | | | –20 | 20 | |
| | | Address, $\overline{WE}$ | | | –20 | 20 | |
| Output Leakage Current | | | 0 V ≤ $V_{OUT}$ ≤ 5.5 V, Data out disabled | $I_{O(L)}$ | –20 | 20 | µA |
| Operating Current (Average Power Supply Current) | *2 | MB8501D032AA-60 | $\overline{RAS}$ & $\overline{CAS}$ cycling, $t_{RC}$ = min | $I_{CC1}$ | — | 320 | mA |
| | | MB8501D032AA-70 | | | — | 300 | |
| Standby Current (Power Supply Current) | *2 | TTL Level | $\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$ | $I_{CC2}$ | — | 4 | mA |
| | | CMOS Level | $\overline{RAS}$ = $\overline{CAS}$ ≥ $V_{CC}$ – 0.2 V | | — | 2 | |
| Refresh Current #1 (Average Power Supply Current) | *2 | MB8501D032AA-60 | $\overline{CAS}$ = $V_{IH}$, $\overline{RAS}$ = cycling, $t_{RC}$ = min | $I_{CC3}$ | — | 320 | mA |
| | | MB8501D032AA-70 | | | — | 300 | |
| Fast Page Mode Current | *2 | MB8501D032AA-60 | $\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$ = cycling, $t_{PC}$ = min | $I_{CC4}$ | — | 200 | mA |
| | | MB8501D032AA-70 | | | — | 180 | |
| Refresh Current #2 (Average Power Supply Current) | *2 | MB8501D032AA-60 | $\overline{RAS}$ = cycling, $\overline{CAS}$-before-$\overline{RAS}$, $t_{RC}$ = min | $I_{CC5}$ | — | 320 | mA |
| | | MB8501D032AA-70 | | | — | 300 | |
| Refresh Current #3 (Average Power Supply Current) | | | Self Refresh | $I_{CC9}$ | — | 2 | mA |

**Notes:** *1. Referenced to $V_{SS}$.

*2. $I_{CC}$ depends on the output load conditions and cycle rate. The specific values are obtained with the output open.
$I_{CC}$ depends on the number of address change as $\overline{RAS}$ = $V_{IL}$ and $\overline{CAS}$ = $V_{IH}$ and $V_{IL}$ > –0.3 V.
$I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC5}$ are specified at one time of address change during $\overline{RAS}$ = $V_{IL}$ and $\overline{CAS}$ = $V_{IH}$.
$I_{CC2}$ is specified during $\overline{RAS}$ = $V_{IH}$ and $V_{IL}$ > –0.3 V.

# MB8501D032AA-60/-70

## ■ AC CHARACTERISTICS

**(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3**

| No. | Parameter | Notes | Symbol | MB8501D032AA-60 | | MB8501D032AA-70 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| 1 | Time between Refresh | | $t_{REF}$ | — | 16.4 | — | 16.4 | ms |
| 2 | Random Read/Write Cycle Time | | $t_{RC}$ | 110 | — | 130 | — | ns |
| 3 | Access Time from $\overline{RAS}$ | *4, 7 | $t_{RAC}$ | — | 60 | — | 70 | ns |
| 4 | Access Time from $\overline{CAS}$ | *5, 7 | $t_{CAC}$ | — | 15 | — | 17 | ns |
| 5 | Column Address Access Time | *6, 7 | $t_{AA}$ | — | 30 | — | 35 | ns |
| 6 | Output Hold Time | | $t_{OH}$ | 3 | — | 3 | — | ns |
| 7 | Output Buffer Turn On DelayTime | | $t_{ON}$ | 0 | — | 0 | — | ns |
| 8 | Output Buffer Turn Off Delay Time | *8 | $t_{OFF}$ | — | 15 | — | 17 | ns |
| 9 | Transition Time | | $t_T$ | 3 | 50 | 3 | 50 | ns |
| 10 | $\overline{RAS}$ Precharge Time | | $t_{RP}$ | 40 | — | 50 | — | ns |
| 11 | $\overline{RAS}$ Pulse Width | | $t_{RAS}$ | 60 | 100000 | 70 | 100000 | ns |
| 12 | $\overline{RAS}$ Hold Time | | $t_{RSH}$ | 15 | — | 17 | — | ns |
| 13 | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | | $t_{CRP}$ | 5 | — | 5 | — | ns |
| 14 | $\overline{RAS}$ to $\overline{CAS}$ Delay Time | *9, 10 | $t_{RCD}$ | 20 | 45 | 20 | 53 | ns |
| 15 | $\overline{CAS}$ Pulse Width | | $t_{CAS}$ | 15 | 10000 | 17 | 10000 | ns |
| 16 | $\overline{CAS}$ Hold Time | | $t_{CSH}$ | 60 | — | 70 | — | ns |
| 17 | $\overline{CAS}$ Precharge Time (C-B-R Refresh) | *16 | $t_{CPN}$ | 10 | — | 10 | — | ns |
| 18 | Row Address Setup Time | | $t_{ASR}$ | 0 | — | 0 | — | ns |
| 19 | Row Address Hold Time | | $t_{RAH}$ | 10 | — | 10 | — | ns |
| 20 | Column Address Setup Time | | $t_{ASC}$ | 0 | — | 0 | — | ns |
| 21 | Column Address Hold Time | | $t_{CAH}$ | 15 | — | 15 | — | ns |
| 22 | Column Address Hold Time from $\overline{RAS}$ | | $t_{AR}$ | 35 | — | 35 | — | ns |
| 23 | $\overline{RAS}$ to Column Address Delay Time | *11 | $t_{RAD}$ | 15 | 30 | 15 | 35 | ns |
| 24 | Column Address to $\overline{RAS}$ Lead Time | | $t_{RAL}$ | 30 | — | 35 | — | ns |
| 25 | Column Address to $\overline{CAS}$ Lead Time | | $t_{CAL}$ | 30 | — | 35 | — | ns |
| 26 | Read Command Setup Time | | $t_{RCS}$ | 0 | — | 0 | — | ns |
| 27 | Read Command Hold Time Referenced to $\overline{RAS}$ | *12 | $t_{RRH}$ | 0 | — | 0 | — | ns |

*(Continued)*

*(Continued)*

| No. | Parameter | Notes | Symbol | MB8501D032AA-60 | | MB8501D032AA-70 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| 28 | Read Command Hold Time Referenced to $\overline{CAS}$ | *12 | $t_{RCH}$ | 0 | — | 0 | — | ns |
| 29 | Write Command Setup Time | *13, 17 | $t_{WCS}$ | 0 | — | 0 | — | ns |
| 30 | Write Command Hold Time | | $t_{WCH}$ | 15 | — | 15 | — | ns |
| 31 | Write Command Hold Time from $\overline{RAS}$ | | $t_{WCR}$ | 35 | — | 35 | — | ns |
| 32 | $\overline{WE}$ Pulse Width | | $t_{WP}$ | 10 | — | 10 | — | ns |
| 33 | Write Command to $\overline{RAS}$ Lead Time | | $t_{RWL}$ | 15 | — | 17 | — | ns |
| 34 | Write Command to $\overline{CAS}$ Lead Time | | $t_{CWL}$ | 15 | — | 17 | — | ns |
| 35 | DIN Setup Time | | $t_{DS}$ | 0 | — | 0 | — | ns |
| 36 | DIN Hold Time | | $t_{DH}$ | 15 | — | 15 | — | ns |
| 37 | Data Hold Time from $\overline{RAS}$ | | $t_{DHR}$ | 35 | — | 35 | — | ns |
| 38 | $\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles) | | $t_{RPC}$ | 5 | — | 5 | — | ns |
| 39 | $\overline{CAS}$ Setup Time (C-B-R Refresh) | | $t_{CSR}$ | 0 | — | 0 | — | ns |
| 40 | $\overline{CAS}$ Hold Time (C-B-R Refresh) | | $t_{CHR}$ | 10 | — | 12 | — | ns |
| 41 | $\overline{CAS}$ to Data in Delay Time | | $t_{CDD}$ | 15 | — | 17 | — | ns |
| 42 | DIN to $\overline{CAS}$ Delay Time | | $t_{DZC}$ | 0 | — | 0 | — | ns |
| 43 | Fast Page Mode $\overline{RAS}$ Pulse Width | | $t_{RASP}$ | — | 100000 | — | 100000 | ns |
| 44 | Fast Page Mode Read/Write Cycle Time | | $t_{PC}$ | 40 | — | 45 | — | ns |
| 45 | Access Time from $\overline{CAS}$ Precharge | *7, 15 | $t_{CPA}$ | — | 35 | — | 40 | ns |
| 46 | Fast Page Mode $\overline{CAS}$ Precharge Time | | $t_{CP}$ | 10 | — | 10 | — | ns |
| 47 | Fast Page Mode $\overline{RAS}$ HoldTime from $\overline{CAS}$ Precharge | | $t_{RHCP}$ | 35 | — | 40 | — | ns |
| 48 | Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time | *17 | $t_{CPWD}$ | 55 | — | 62 | — | ns |
| 49 | $\overline{RAS}$ Pulse Width (Self Refresh) | *18 | $t_{RASS}$ | 100 | — | 100 | — | µs |
| 50 | $\overline{RAS}$ Precharge Time (SelfRefresh) | *18 | $t_{RPS}$ | 110 | — | 125 | — | ns |
| 51 | $\overline{CAS}$ Hold Time (Self Refresh) | *18 | $t_{CHS}$ | –50 | — | –50 | — | ns |

# MB8501D032AA-60/-70

**Notes:** *1. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{CAS}$- before-$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.

*2. AC characteristics assume $t_T$ = 5 ns.

*3. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measureing the timing of input signals. Transition times are measured between $V_{IH}$ (min) and $V_{IL}$ (max).

*4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If $t_{RCD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will be increased by the amount that $t_{RCD}$ exceeds the value shown.

*5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is $t_{CAC}$.

*6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is $t_{AA}$.

*7. Measured with a load equivalent to two TTL loads and 100 pF.

*8. $t_{OFF}$ and $t_{OEZ}$ are specified that output buffer change to high-impedance state.

*9. Operation within the $t_{RCD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, access time is controlled exclusively by $t_{CAC}$ or $t_{AA}$.

*10. $t_{RCD}$ (min) = $t_{RAH}$ (min)+ $2t_T$ + $t_{ASC}$ (min).

*11. Operation within the $t_{RAD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RAD}$ (max) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, access time is controlled exclusively by $t_{CAC}$ or $t_{AA}$.

*12. Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for a read cycle.

*13. $t_{WCS}$ is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.

*14. Assumes that $t_{WCS} < t_{WCS}$ (min).

*15. $t_{CPA}$ is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if $t_{CP}$ become long, $t_{CPA}$ also become longer than $t_{CPA}$ (max).

*16. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.

*17. $t_{WCS}$ and $t_{CPWD}$ are not restrictive operating parameters.They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and $D_{OUT}$ pin will maintain high-impedance state thoughout the entire cycle. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the $D_{OUT}$ pin, and write operation can be executed by satisfying $t_{RWL}$, $t_{CWL}$, $t_{RAL}$ and $t_{CAL}$ specifications.

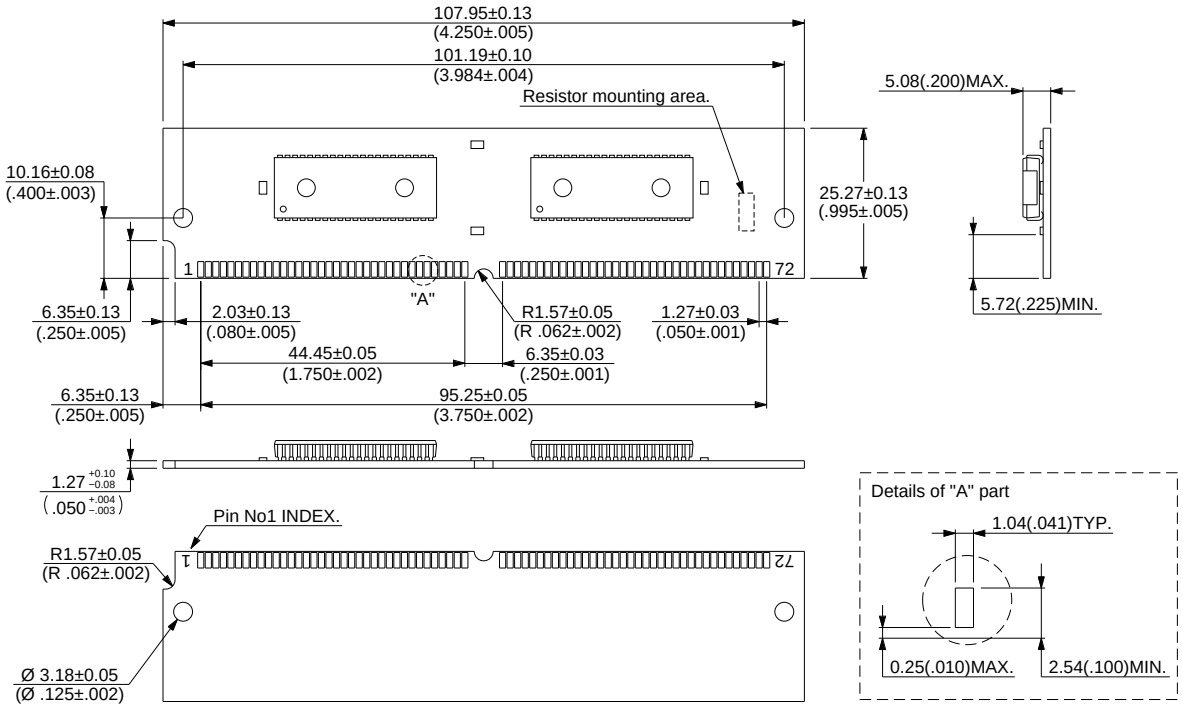
*18. Assumes that self refresh.

*Source: See MB8118160A Data Sheet for details on the electricals.

# MB8501D032AA-60/-70

## ■ PACKAGE DIMENSIONS

**72-PIN SINGLE IN-LINE MEMORY MODULE**
**(CASE No.: MSS-72P-P86)**






Dimensions in mm (inches)

# MB8501D032AA-60/-70

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